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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/353,998	07/15/1999	SUSUMU SENSYU	SONY-P9817	4457

22850 7590 01/26/2005

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EXAMINER	
SHAH, NILESH R	

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/353,998	SENSYU, SUSUMU	
	Examiner	Art Unit	
	Nilesh Shah	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-12 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-12, 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 –26 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   A) The following claim language is not clearly define:

   a) As per claim 1, lines 9-10 it is unclear what the processor is associated with which switching queue (i.e. is there a predetermine method of associating each processor with each switching queue?; line 11, is the task a new task?; lines 15-16, it is unclear what is meant by "a one of said each said one instruction processor's associated switching queue" (i.e is there some information associated with the switching queue to identify which processor?); line 18 what is the second level switching queue? Is there a first level? What is the difference between the first and second levels?; line 20, when does the inquiring take place? Before the second level?

b) Claim 17 has similar problems as to claim 1 above.

c) As per claim 18, line 13, it is unclear what "substantially the same number as instruction processors" means. The number of instruction processor is not set therefore it is unknown the number of switching queues; lines 14-15, a one of said each said one instruction processor's associated switching queue (i.e is there some information associated with the switching queue to identify which processor?).

d) Claims 22 and 23 have similar problems as claim 18 above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

   a. A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steely et al (6,088,771) (hereinafter Steely) in view of Gove et al (5,220,777) (hereinafter Gove).

6. As per claim 1, Steely teaches the invention substantially as claimed including a method for assigning to and ordered executing of tasks by instruction processors in a multiple instruction processor computer system having at least three levels of memory(col. 5 lines 1-22), said at least three levels being at least two cache levels(col. 5 lines 24-37), a first

of which is accessible directly by a single one of said instruction processors(col. 6 lines 45-51), a mid-level memory being a multiprocessor-accessible cache accessible by at least two of said instruction processors(col. 2 lines 12-16), and a third memory level being a main memory, accessible by all of said instruction processors(col. 2 lines 32-40), said method comprising:

assigning said task to said selected switching queue by placing information about an affined switching queue into said new task running a one of said instruction processors based upon tasks (col. 4 lines 20-30) having information in said one instruction processor's associated switching queue until there are no tasks in a one of said each said one instruction processor's associated switching queue and then(col. 10 lines 47-56; col.3 lines 47-50).

7. Steely does not specifically teach the following limitations.

Gove teaches selecting a processor-associated switching queue to which to assign a new task (col. 37 lines 60-67;col. 47 lines 35-43);

determining through the use of a selection matrix which other switching queue may be used as a second level switching queue by said one instruction processor(col. 5 lines 20-34); and

inquiring by said one instruction processor of said second level switching queue for a next task that may be available on said second level switching queue.(col. 5 lines 49-63). It would have been obvious to one skill in the art at the time of the invention to combine the teachings of Gove and Steely because Gove's method of using the switching queue

for new tasks would improve Steely's system by making it easier and more efficient for new tasks to enter the queue.

8. As per claim 2, Steely teaches a method wherein if said second switching queue has a said next task, assigning affinity for that task to said one instruction processor and allowing said one instruction processor to execute said next task (col. 4 lines 20-33; col. 5 lines 14-22).

9. As per claim 3, Gove teaches a method wherein said selection matrix provides a hierarchical selection agenda through which access to a new switching queue is determined when said one instruction processor's associated switching queue (col. 5 lines 20-34) has no tasks and wherein said hierarchical selection agenda first selects said second level switching queue from among switching queues associated with instruction processors on a same bus as said one instruction processor (col. 37 lines 60-67;col. 47 lines 35-43).

10. As per claim 4, Gove teaches a method wherein after said hierarchical selection agenda first selects said second level switching queue from among switching queues associated with instruction processors on a same bus as said one instruction processor(col. 6 lines 37-55), if said one instruction processor cannot find a said next task on said second level switching queue, said hierarchical selection agenda then selects a third level switching

queue from among switching queues associated with instruction processors that use a shared cache with said one instruction processor (col. 5 lines 20-34).

11. As per claim 5, Steely teaches a method wherein after said hierarchical selection agenda selects said third level switching queue from among switching queues associated with instruction processors on a shared cache shared with said one instruction processor(col. 5 lines 24-37), if said one instruction processor cannot find a said next task(col. 6 lines 45-51), on said third level switching queue, said hierarchical selection agenda then selects a fourth level switching queue from among switching queues associated with instruction processors that use a crossbar with said one instruction processor (col. 4 lines 20-33; col. 5 lines 14-22).

12. As per claim 6, Steely teaches a method wherein after said hierarchical selection agenda selects said fourth level switching queue from among switching queues associated with instruction processors on a shared cache shared with said one instruction processor(col. 5 lines 24-35), if said one instruction processor cannot find a said next task on said fourth level switching queue, said hierarchical selection agenda then selects from among switching queues associated with instruction processors that use another crossbar to access main memory than the one used by said one instruction processor (col. 10 lines 47-56).

13. As per claim 7, Gove teaches a method wherein said information queue is placed as header information into said new task about said switching (col. 37 lines 60-67;col. 47 lines 35-43).

14. As per claim 8, Gove teaches a method further comprising monitoring busyness of an instruction processor to determine whether to proceed to said inquiring step or to idle said instruction processor and only proceeding to said inquiring step where said monitored busyness reaches a threshold value (col. 51 lines 18-35)

15. As per claim 9, Gove teaches a method wherein said monitoring comprises periodically checking the busyness of instruction processors (col. 16 lines 20-42).

16. As per claim 10, Gove teaches a method wherein said monitoring comprises periodically checking the busyness of each of said instruction processors (col. 16 lines 20-42).

17. As per claim 11, Gove teaches a method further comprising evaluating the relative busyness of said one instruction processor to all others of said instruction processors (col. 9 lines 55-67; col. 16 lines 20-42).

18. As per claim 12, Gove teaches a method wherein said threshold value is set differently for different levels of switching queues (col. 9 lines 55-67; col. 16 lines 20-42).

19. As per claim 13, Gove teaches a method wherein said selecting of a processor-associated switching queue to which to assign a new task is based upon idleness qualities of all available processor-associated switching queues (col.12 lines 60-68)

20. As per claim 14, Gove teaches a method wherein said selecting of a processor-associated switching queue to which to assign a new task may accomplished using substantially any one of said instruction processors of said multiple instruction processors (col.12 lines 60-68; col. 16 lines 20-42).

21. As per claim 15, Steely teaches a method wherein said selecting of a processor-associated switching queue to which to assign a new task may accomplished using substantially every one of said instruction processors of said multiple instruction processors, as each of said substantially every one of said instruction processors becomes ready to seek a new task (col. 4 lines 20-33; col. 5 lines 14-22).

22. As per claim 16, Gove teaches a method wherein said selecting of a processor-associated switching queue to which to assign a new task assigns said task to a switching queue used by a plurality of said instruction processors for their processor- associated switching queue (col. 37 lines 60-67;col. 47 lines 35-43).

23. Claim 17 is rejection based on the same rejection as claim 1 above.

24. As per claim 18, Steely teaches a dispatcher algorithm for use in a multiple instruction processor computer system having at least three levels of memory(col. 5 lines 1-22),, said three levels being at least two cache levels(col. 5 lines 24-37),, a first of which is accessible directly by a single one of said instruction processors(col. 6 lines 45-51),, a mid-level memory being a multiprocessor-accessible cache accessible by at least two of said instruction processors(col. 2 lines 12-16),, and a third memory level being a main memory, accessible by all of said instruction processors, wherein tasks are directed to switching queues for processor assignment on an affinity basis by an executive and said switching queues are maintained and controlled by said dispatcher algorithm, said dispatcher algorithm (col. 2 lines 32-40) comprising:

a set of switching queues of substantially the same number as instruction processors wherein one switching queue is associated with said one of said instruction processors(col. 4 lines 20-30) and a switching queue is also associated with substantially each other of said instructions processors, said switching queues having code for their operation and a data area wherein said data area is for maintaining a list of tasks for an instruction processor to accomplish (col. 10 lines 47-56; col.3 lines 47-50).

Gove teaches an executable program for assigning affinity of each new task to a one of said instruction processors executing said executable program (col. 37 lines 60-67;col. 47 lines 35-43); and

a load balancing level matrix for directing said first instruction processor to steal a task from a switching queue (col. 5 lines 20-34) associated with another instruction processor

in accord with a predetermined mapping within said matrix when said first instruction processor is looking for an additional task (col. 37 lines 60-67;col. 47 lines 35-43).

25. As per claim 19, Gove teaches an apparatus additionally comprising a monitor program for measuring a level of instruction processor busyness/idleness of said one instruction processor, for comparing the level of busyness/idleness to a predetermined threshold(col. 9 lines 55-67; col. 16 lines 20-42), and if the measured level of busyness/idleness exceeds the threshold, for permitting said one instruction processor to use the load balancing level matrix to determine which of said other instruction processor-associated switching queues to seek a new task from (col. 37 lines 60-67;col. 47 lines 35-43).

26. As per claim 20, Gove teaches an apparatus wherein said monitor operates as executable code of the dispatcher algorithm used by an instruction processor when said instruction processor seeks a new task wherein a value related to a current level of busyness of said instruction processor using said monitor executable code is stored in an instruction processor busyness data area (col. 9 lines 55-67; col. 16 lines 20-42).

27. As per claim 21, Gove teaches an apparatus wherein said monitor evaluates the values stored in said instruction processor busyness data area and generates a level of busyness value of the multiprocessor system there-from, and based on a comparison between said current busyness value for this one instruction processor(col. 9 lines 55-67; col. 16 lines 20-42), produces a transfer affinity value, and wherein said monitor compares said

transfer affinity value against a threshold level value to determine whether said another instruction processor will be permitted to steal a task from said one instruction processor-associated switching queue or not(col. 37 lines 60-67;col. 47 lines 35-43).

28. Claims 22-23 are rejected based on the same rejection as claim 18 above.

29. As per claim 24, Steely teaches a multiple instruction processor computer system having a dispatcher algorithm (col. 10 lines 47-56; col.3 lines 47-50).

30. As per claim 25, Steely teaches a dispatcher algorithm wherein each said processor unit comprises either a cluster of instruction processors or a single instruction processor (col. 4 lines 57-67).

31. As per claim 26, Steely teaches a dispatcher algorithm wherein at least one of said processor units is comprised of a different number of instruction processors than at least one other one of said processor units (col. 4 lines 57-67).

Conclusion

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nilesh Shah whose telephone number is (571)272-3771. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nilesh Shah
Examiner
Art Unit 2127

NS
January 19, 2005

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